REMARKS

Claims 18-25 are currently pending. Claims 1-17 were previously cancelled. Applicant reserves the right to pursue original and other claims in this and in other applications.

The Drawings stand objected to for FIG. 6 allegedly not being "an accurate representation of applicant's claimed invention because figure 6 is actually too small in scale to clearly show the claimed subject matter." Applicant respectfully traverses the objection and respectfully submits that FIG. 6 shows an image sensor including a pixel section and a decoder section. FIG. 6 is one of several figures used to describe, in an example fashion, the claimed invention. FIG. 6 is used to highlight an interconnect layout for use in decoder block including stitched blocks according to an embodiment. Thus, the alleged small scale does not detract or fail to disclose claimed features. Thus, the rejection of the drawings should be withdrawn.

Claims 18-25 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

With respect to claims 18 and 21, the Office states:

> Applicant claims pixel and decoder sections (having routing lines) as having first and second pitches. Does [A]pplicant intend to mean the pitch of the entire sections, for example, the pitch between pixel elements and decode elements or does [A]pplicant mean to claim the pitch of the routing lines?

Applicant suggests that the claims are clear and definite and indicate that both the pixel and decoder sections "having" a first and second pitch, respectively. As the term "having" is used, the Applicant intends that the features of the elements have a particular pitch. Thus, the rejection of claims 18 and 21 should be withdrawn.

With respect to claim 21, the Office states:

> Applicant claims 'wherein said features include routing lines', but does not clarify whether or not lines apply to the decoder section, the pixel section or both sections.

Applicant suggests that the claims are clear and definite and indicate that both the pixel and decoder sections have routing lines. Thus, the rejection of claim 21 should be withdrawn.

Claims 18, 21-22, and 24 stand rejected under 35 U.S.C. 102(b) as being anticipated by Cazaux (U.S. Pat. No. 5,777,672). Applicant respectfully traverses the rejection.

Claim 18 recites:

> An image sensor comprising:
>
> a pixel section of the image sensor including routing lines, said pixel section having a first pitch, and
>
> a decoder section of said image sensor including routing lines, said decoder section having a second pitch,
>
> wherein the second pitch is smaller than the first pitch.

Cazaux discloses:

> ...a CCD type photosensitive device, the charges produced in two consecutive columns of pixels are transferred into different reading registers: the charges from the first column are loaded into the first register and the charges from the second column travel through the first register to be loaded into the second register. The two reading registers are controlled by independent potentials during the step for the loading of these registers. The device makes it possible to increase the efficiency of the transfer between the two reading registers, especially when the registers are of the type working in a two-phase mode.

(Cazaux, abstract)

The Office suggests that Cazaux' FIG. 2, reproduced below, reads on the claimed invention. P1 are pixel sections and PE1, PE2, of RL1 or RL2 (alleged to be decoder sections) are reading elements. (Cazaux, Col. 5, lines 43-58).

The Office further notes that:

> Cazaux shows the CCD as an image sensor , and the reading registers as decoders. The reading registers are decoders because they take signals from the pixel section, shift the information into the reading register, and output the information in a serial manner. Further [A]pplicant does not explain or claim what the decoder is and therefore the reading elements of Cazaux read on the claimed invention.

A decoder, as is conventionally known in the context of image sensor, is generally understood to be a device that translates an address into an implementation of an address. For example, a row decoder receives an address corresponding to a particular row and decodes the address information and provides the appropriate signals to enable the designated row.

Contrary to the suggestion of the Office, Cazaux's reading registers are not decoders. Cazaux's reading registers are shift registers that receive signals from pixels in a CCD image sensor and are used to shift the signals in a transfer direction. Thus, enabling signals to be read out from a CCD image sensor.

Thus, Cazaux's reading registers are different from the decoders of the claim invention and the rejection of claim 18 and its dependant claims in view of Cazaux should be withdrawn.

Claim 21 recites

> A method comprising:
>
> patterning a pixel section of an image sensor including pixel features having a first pitch on a surface; and
>
> patterning a decoder section of the image sensor including features having a second pitch which is smaller than the first pitch on the surface, wherein said features include routing lines.

As noted above, Cazaux's reading registers are different from the decoders of the claim invention and the rejection of claim 21 and its dependant claims in view of Cazaux should be withdrawn.

Claims 18-22 and 24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou (U.S. Pat. No. 5,909,026) in view of Hayano (U.S. Pat. No. 5,195,053). Applicant respectfully traverses the rejection.

Zhou discloses:

> An image sensor operable to vary the output spatial resolution according to a received light level while maintaining a desired signal-to-noise ratio. Signals from neighboring pixels in a pixel patch with an adjustable size are added to increase both the image brightness and signal-to-noise ratio. One embodiment comprises a sensor array for receiving input signals, a frame memory array for temporarily storing a full frame, and an array of self-calibration column integrators for uniform column-parallel signal summation. The column integrators are capable of substantially canceling fixed pattern noise.

(Zhou, Abstract)

As noted by the Office, Zhou fails to disclose that "wherein the second pitch is smaller than the first pitch."

Hayano discloses that:

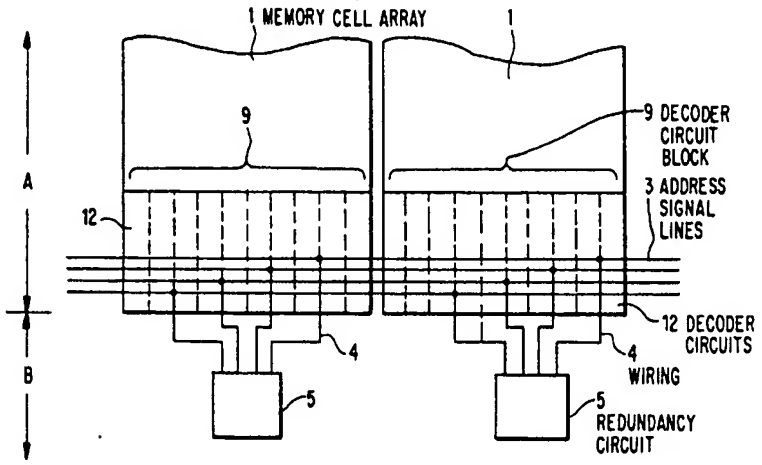
> a plurality of address signal lines are formed in an upper wiring layer, the plurality of decoder circuits are formed by circuit elements interconnected by a wiring layer in a lower level than the address signal lines and arranged with the same pattern as that of the decoder circuits. A first boundary region of a predetermined width is provided between one decoder circuit pattern and another decoder circuit pattern adjacent to one side of the one decoder circuit pattern, a wider, second boundary region is provided between the one decoder circuit pattern and another decoder circuit pattern adjacent to the other side of the another decoder circuit pattern and wires connecting the

address wirings to peripheral circuits are provided in the second boundary region in a level lower than the address wiring level.

(Hayano, abstract)

The Office suggests that Hayano's FIG. 6, reproduced below, reads on the claimed invention.

FIG. 6



The Office likens "a pixel section...having a first pitch, and a decoder section...having a second pitch" to Hayano's pixel array 1 and decoder circuits 12. However, the Office fails to properly show how Hayano is to be applied and only identifies the two elements, but does not suggest or identify how these two elements correspond to the claimed features. The Office fails to indicate how the pixel array 1 has a pitch, where pixel array 1 does not seem to have any inclusive elements, and thus fails to indicate how it would have a larger pitch than the decoder circuits, which the Office has also not identified the correspondence with the claimed invention's decoder section.

Thus, although the Office suggests that:

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Zhou and

Hayano because adding Hayano's decoder section with a smaller pitch, stitched together in series, and having pitch's of less than approximately 0.98 and 0.95 would have been advantageous for Zhou's image sensor and method for patterning pixel and decoder sections to have a decoder section with a smaller pitch because having the smaller pitch would allow for a larger image sensor to be addressed while reducing overall area of the device, which reduce the cost of the device.

Without the Office providing an indication of how the features of elements of Hayano compare to the claimed invention, the reference is inapplicable. Thus, the rejection of the claims based on Hayano should be withdrawn.

In view of the above, Applicant believes the pending application is in condition for allowance.

Dated:

Respectfully submitted,

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